WHAT IS CLAIMED IS:

1. A fuse box, comprising:

a plurality of make-links for programming an address of a defective normal memory cell with an address of a corresponding redundant memory cell.

2. The fuse box of claim 1, wherein the address of the defective normal memory cell and the address of the corresponding redundant memory cell are row addresses or column addresses.

3. A fuse box, comprising:

a plurality of make-links for replacing a defective normal bit line with a corresponding redundant bit line.

4. A fuse box, comprising

a plurality of make-links for replacing a defective normal word line with a corresponding redundant word line.

5. A redundant address decoder, comprising:

a fuse box including a plurality of make-links for decoding an address of a defect cell; and

a redundant word line selection circuit for selecting a word line of a redundant cell corresponding to the address of the defect cell in response to a signal output from the fuse box.

6. The redundant address decoder of claim 5, wherein each of the make-links includes a first end and a second end, and the redundant address decoder further comprises:

a plurality of transistors, each of the plurality of transistors having a source connected to the first end of one of the plurality of make-links;

a plurality of nodes, each of the plurality of nodes connected to the second end of one of the plurality of make-links.

7. The redundancy address decoder of claim 6, wherein the redundant word line selection circuit comprises:

an inverter connected to a first one of the plurality of nodes for performing an inversion operation;

a first NAND gate connected to second and third ones of the plurality of nodes for performing a NAND operation;

a second NAND gate connected to fourth and fifth ones of the plurality of nodes for performing the NAND operation;

a NOR gate connected to the inverter, the first NAND gate, and the second NAND gate for performing a NOR operation.

8. The redundancy address decoder of claim 7, wherein each of the plurality of transistors have a gate connected to a redundancy enable signal.

9. The redundancy address decoder of claim 8, further comprising another plurality of nodes for receiving defect cell addresses, wherein each of the plurality of transistors has a drain connected to one of the other plurality of nodes.

10. A redundant address decoder, comprising:

a fuse box including a plurality of make-links for decoding an address of a defect cell; and

a redundant bit line selection circuit for selecting a bit line of a redundant cell corresponding to the address of the defect cell in response to a signal output from the fuse box.

11. The redundant address decoder of claim 10, wherein each of the make-links includes a first end and a second end, and the redundant address decoder further comprises:

a plurality of transistors, each of the plurality of transistors having a source connected to the first end of one of the plurality of make-links;

a plurality of nodes, each of the plurality of nodes connected to the second end of one of the plurality of make-links.

12. The redundancy address decoder of claim 11, wherein the redundant word line selection circuit comprises:

an inverter connected to a first one of the plurality of nodes for performing an inversion operation;

a first NAND gate connected to second and third ones of the plurality of nodes for performing a NAND operation;

a second NAND gate connected to fourth and fifth ones of the plurality of nodes for performing the NAND operation;

a NOR gate connected to the inverter, the first NAND gate, and the second NAND gate for performing a NOR operation.

13. The redundancy address decoder of claim 12, wherein each of the plurality of transistors have a gate connected to a redundancy enable signal.

14. The redundancy address decoder of claim 13, further comprising another plurality of nodes for receiving defect cell addresses, wherein each of the plurality of transistors has a drain connected to one of the other plurality of nodes.

15. A method for repairing a defective memory cell, comprising the steps of:

receiving an address of the defective cell;

decoding the address of the defective cell through make-links; and

selecting a redundant word line corresponding to the address of the defective cell and replacing the defective cell with a redundant cell.